Q.P. Code: 16CS506 **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

BTECH II Year I Semester Supplementary Examinations Nov/Dec 2019

DIGITAL LOGIC DESIGN

(CSE & CSIT)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	**a**	Convert the following to binary and then to gray code $(AB33)_{16}$	**6M**
	b	Perform the following Using BCD arithmetic $(7129)_{10} + (7711)_{10}$	**6M**
		OR	
2	**a**	Obtain the Complement of Boolean Expression i) A+B+A'B'C ii) AB + A (B +C) + B'(B+D)	**6M**
	b	Explain the Excess-3 code with any two examples.	**6M**

UNIT-II

3		Obtain the minimal product of sums and design using NAND gates $F(A,B,C,D)= \sum m(0,2,3,6,7) + d(8,10,11,15)$	**12M**
		OR	
4		Simplify the Boolean expression using K-MAP $F(A,B,C,D) = \pi M (3,5,6,7,11,13,14,15) .d(9,10,12)$	**12M**

UNIT-III

5	**a**	Explain about Binary Half Adder?	**6M**
	b	What is Full Adder? And Explain the operations of Full Adder?	**6M**
		OR	
6		Implement BCD to 7-segment decoder for common anode using 4:16 decoder?	**12M**

UNIT-IV

7	**a**	Draw and explain the operation of T Flip-Flop?	**6M**
	b	Explain about Ring counter & Ripple Counter.	**6M**
		OR	
8		Explain the design of a 4 bit binary counter with parallel load in detail?	**12M**

UNIT-V

9		What is memory decoding? Explain about the construction of 4 X 4 RAM?	**12M**
		OR	
10		Construct the PLA using the conversion from BCD code to Excess-3 code?	**12M**

*** END ***